REMARKS

Claim Rejections - 35 U.S.C. §103

Claims 1-10 are rejected under 35 USC §103(a) as being unpatentable over Kitamura in view of Kalagnanam et al. (U.S. Patent No. 6,044,361).

Independent claim 1 is supported by way of an example in Figures 3-4 and 7-9 and associated written specification, wherein there is indeed disclosed a manufacturing system (Figures 2-3, 5, product control system A) for manufacturing printed wiring boards of plural types, said printed wiring boards scheduled to be manufactured are laid out on at least one predetermined manufacturing block (Figures 7, 9, 11), comprising:

a schedule data storage unit (Figs. 3-4, 32) storing manufacturing schedule data (Figs. 3-4, 36) including printed wiring board data, each type of the printed wiring boards and a number of each of the printed wiring boards scheduled to be manufactured;

a detecting unit (Figs. 3, 5, 31; Figs. 6-7, S103) detecting a plurality of fractional printed wiring boards (Figures 7 and 9, appendix) which should be laid out to a format of a single predetermined manufacturing block together with a plurality of printed wiring boards having a different type (Fig. 9) within the printed wiring boards scheduled to be manufactured based on the manufacturing schedule data stored in said schedule data storage unit (printed wiring board data of Fig. 3, reference numeral 35 and predetermined manufacturing block data of Fig. 3, reference numeral 34) printed wiring board data, and predetermined manufacturing block data;

a condition data storage unit (Fig. 3, 32) storing manufacturing condition data (Fig. 3, reference numeral 37-38) for laying out printed wiring boards of the plural types on a format of a

single predetermined manufacturing block;

a grouping unit (Figure 3, 31; Figs. 6 and 8, S104, S201, S202, S203) grouping each of the fractional printed wiring boards detected by said detecting unit into any of a number of groups according to the manufacturing condition data stored in said condition data storage unit; and

a determining unit (Figure 3, 31; Figs. 6 and 9, S105) determining, per group, layout to the at least one predetermined manufacturing block of the fractional printed wiring board.

Independent claim 9 is supported by way of an example in Figures 3-4 and 7-9 and associated written specification, wherein there is indeed disclosed a manufacturing method for manufacturing printed wiring boards of plural types, said printed wiring boards scheduled to be manufactured are laid out to at least one predetermined manufacturing block, comprising:

reading manufacturing schedule data (Fig. 6, S101) including printed wiring board data, each of the plural types of the printed wiring boards and a number of each of the printed wiring boards scheduled to be manufactured;

detecting a plurality of fractional printed wiring boards (Fig. 6, S103) which should be laid out to a format of a single predetermined manufacturing block together with a plurality of printed wiring boards having a different type within the printed wiring boards scheduled to be manufactured based on the manufacturing schedule data (printed wiring board data of Fig. 3, reference numeral 35, and predetermined manufacturing block data of Fig. 3 reference numeral 34);

reading a manufacturing condition data (Fig. 6 and 8, S104) for laying out printed wiring boards of the plural types on a format of a single predetermined manufacturing block;

grouping (Fig. 6 and 8, S104) each of the detected fractional printed wiring boards into any of a number of groups according to the manufacturing condition data (Fig. 3, 37-38); and

determining, per group, layout to the at least one predetermined manufacturing block of the fractional printed wiring board (Figs. 6 and 9, S105).

Independent claim 10 is supported by way of an example in Figures 3-4 and 7-9 and associated written specification, wherein there is indeed disclosed a computer-readable recording medium (Fig. 3, 32) for recording a computer program for making a computer to carry out processes for manufacturing printed wiring boards of plural types, said printed wiring boards scheduled to be manufactured are laid out to at least one predetermined manufacturing block (Figs. 7, 9, 11), the program comprising:

reading manufacturing schedule data (Fig. 6, S101) including printed wiring board data, each of the plural types of the printed wiring boards and a number of each of the printed wiring boards scheduled to be manufactured;

detecting a plurality of fractional printed wiring boards (Fig. 6, S103) which should be laid out to a single predetermined manufacturing block together with a plurality of printed wiring boards having a different type within the printed wiring boards scheduled to be manufactured based on the multiple manufacturing schedule data (printed wiring board data of Fig. 3, 35 and predetermined manufacturing block data of Fig. 3, 34);

reading manufacturing condition data (Figs. 6, 8, S104) for laying out printed wiring boards of the plural types to a format of a single predetermined manufacturing block;

grouping each of the detected fractional printed wiring boards into any of a number of

groups (Figs. 6 and 8, S104) according to the manufacturing condition data; and

determining, per group, layout to the at least one predetermined manufacturing block of the fractional printed wiring board (Figs 6 and 9, S105).

In rejecting the claimed invention, the outstanding Office action has positively stated that "Kitamura does not expressly disclose handling fractional printed circuit boards or fractional groups of printed circuit boards." The Applicant agrees with this Office assessed shortcoming of Kitamura.

To supplement this shortcoming, the Office asserted a secondary reference Kalagnanam stating that "Kalagnanam et al. discloses handling fractional items in a manufacturing system with inventory matching." The Office then cited certain column and line numbers.

It should be noted that while the Applicant has no quarrels that "Kalagnanam et al. discloses handling fractional items in a manufacturing system with inventory matching", it is not understood how this fact supplement to the Office assessed shortcoming that "Kitamura does not expressly disclose handling fractional printed circuit boards or fractional groups of printed circuit boards."

In fact, Kalagnanam et al. fails to even mention the term "circuit board", naturally, Kalagnanam et al. would not provide any disclosure or teaching of "handling fractional printed circuit boards or fractional groups of printed circuit boards."

In addition to the above-mentioned shortcomings, it should also be noted that independent claims 1 , 9 and 10 has already specified that:

(1) the detecting unit detects a fractional printed wiring board within the printed wiring

boards that manufacture is scheduled. The fractional printed wiring board is laid out to a predetermined manufacturing block together with a printed wiring board of different type;

(2) the grouping unit groups each detected fractional printed wiring board into any of groups depending on the manufacturing condition data;

(3) the determining unit determining layout to at least one predetermined manufacturing block of the fractional printed wiring board belonging to each group.

The outstanding Office action asserts that the system and the central processor of Kitamura respectively correspond to the detecting unit, the grouping unit and the determining unit of the present invention. However, Kitamura does not disclose and teach features (l)-(3) as recited in amended Claims 1 , 9 and 10. Therefore, the claimed invention is already patentably distinguish over the asserted prior art.

Furthermore, the Office fails to establish a *prima facie* case of obviousness, section 2143 of the MPEP has specifically stated that:

> "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference must teach or suggest all the claimed limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 466, 20 USPQ2d 1438 (Fed. Cir. 1991)."

Therefore, it is both a court position and a Patent Office position that to establish a *prima facie* case of obviousness, 1) there **must be** some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the

reference or to combine reference teachings; 2) there **must be** a reasonable expectation of success; and 3) the teaching or suggestion to make the claimed combination and the reasonable expectation of success **must both be** found in the prior art, and not based on applicant's disclosure.

Should the Office finds other prior art references but is either unable to identify each and every aspect of the above-mentioned claimed features therein, or the formulated rejection simply would not rise to a level objectively fulfilling all three criteria of establishing a *prima facie* case of obviousness, it is respectfully submitted that the obviousness rejection would be defective and allowance of the claimed invention is requested.

CONCLUSION

In view of the aforementioned amendments and accompanying remarks, all pending claims are believed to be in condition for allowance, which action, at an early date, is requested.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 50-2866.

Respectfully Submitted,

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